Express Mail No. EK934964652US Date Mailed January 22, 2002

APPLICATION FOR UNITED STATES PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

Honeywell Case No. A11-26110

(MBHB Case No. 00-696)

Title: **HIGH DENSITY 3-D INTEGRATED CIRCUIT PACKAGE**

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High Density 3-D Integrated Circuit Package

GOVERNMENT RIGHTS

The United States Government has acquired certain rights in this invention pursuant to Contract No. DASG60-90-C-0136 awarded by the U.S. Army.

FIELD

The present invention relates generally to circuit packages, and more particularly, relates to three-dimensional circuit packages that provide stacking for semiconductor platelets.

BACKGROUND

Three-dimensional integrated circuits are employed in applications in which space is a critical design factor. As the demand for more functionality in less space increases, so does the number of designs using three-dimensional packaging. In addition to the benefit of reducing space, these designs may also realize higher speeds because interconnects between circuit components may be shorter.

Memory stacking was the first application of three-dimensional packaging, but now applications range from stacking memory modules to stacking entire systems. Different layers in the stack may have different functionalities. For example, one layer may be a memory layer and another may be a logic layer. It is also possible that the different layers in the stack could have different dimensions.

These applications may require the precise stacking of very thin platelets into cubes. Platelets may consist of a semiconductor chip placed in a chip carrier. The platelets themselves may be less than 5 mils thick and there may be as many as sixty platelets stacked in one cube. It is critical that the spacing between the platelets is held to a very tight tolerance and that the platelets are not damaged during the stacking procedure.

Typically, the platelets are held in the cubical stack by a very thin layer of epoxy resin between each layer. This epoxy layer may be less than one micron thick. Other bonding materials, such as silicone rubber or eutectic solder alloy, may also be employed. The required spacing dimensions may be maintained by using an apparatus with a calibrated compression arm that applies pressure to the stack while the epoxy is setting. A typical amount of pressure may be ten Newtons of force. With this arrangement, only the overall cube dimensions can be maintained, and great care must be taken to prevent cracking the delicate platelets by excessive pressure. The critical layer to layer spacing is thus a derived property and is based upon the uniformity of the thickness and pressure-flow characteristics of the adhesive layer.

It would be desirable to provide a stacking method that provides a very tight spacing tolerance between the platelets and that minimizes damage to the platelets during the stacking process. The invention addresses current limitations and makes the critical spacing a directly controlled property resulting in much higher accuracy potential with a relative independence of the adhesive layers.

SUMMARY

In accordance with this invention, a method for stacking semiconductor platelets in a three-dimensional circuit package is described. Three walls are connected to form a slotted file. The two side walls have grooves. The grooves on the two walls face directly across from each other. Placing a semiconductor chip into a frame of a chip carrier forms a platelet. The frame is located on the surface of a floor of the chip carrier. The floor protrudes past the sides of the frame forming flanges on each side of the frame. The flanges fit into the groves of the slotted file. The platelets are then inserted into the slotted file forming a completed cube.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments are described below in conjunction with the appended drawing figures, wherein like reference numerals refer to like elements in the various figures, and wherein:

Fig. 1 is an illustration of an exemplary embodiment of a chip carrier and a semiconductor chip;

Fig. 2 is an illustration of an exemplary embodiment of a slotted file wall;

Fig. 3 is an illustration of an exemplary embodiment of a slotted file;

Fig. 4 is an illustration of the stacking process in an exemplary embodiment; and

Fig. 5 is an illustration of an exemplary embodiment of a completed cube.

DETAILED DESCRIPTION

Fig. 1 is an illustration of an exemplary embodiment of a chip carrier 100 and a semiconductor chip 108. The chip carrier 100 is composed of a floor 102 and a frame 104. The chip carrier 100 may be designed to hold the semiconductor chip 108. The floor 102 may be a three-dimensional rectangle having a length, a width, and a thickness. The frame 104 may be a three-dimensional rectangle with a smaller three-dimensional rectangular center removed. The frame 104 has a length, a width, and a thickness. The frame 104 is substantially the same length as the floor 102; however, the frame 104 is not as wide as the floor 102.

The frame 104 is positioned in the center of the floor 102. Because the width of the floor 102 is greater than the width of the frame 104, the floor 102 protrudes past the edges of the frame 104 forming two flanges 106, one on either side of the frame 104.

In an exemplary embodiment both the floor 102 and the frame 104 are formed with ceramic materials, but other materials such as metal and plastic may be used. The floor 102 contains a plurality of electrodes. The frame 104 has interior dimensions slightly larger than those of the semiconductor chip 108. The interior dimensions of the frame 104 may vary to accommodate a variety of different semiconductor chip 108 dimensions. The semiconductor chip 108 may be placed in the frame 104 face down on the floor 102 contacting the plurality of electrodes at the appropriate circuit interfaces to form a platelet 404 (see Fig. 4).

Fig. 2 is an illustration of a slotted file wall 200. A slotted file wall 200 consists of a wall material 202 and may include a plurality of grooves 204. The wall material 202

may be a three-dimensional rectangle having a length, a width, and a thickness. Silicon is the preferred wall material 202 in an exemplary embodiment, but other materials, such as gallium arsenide, may be used.

The wall material 202 may be etched with grooves 204 deep enough to receive the flanges 106 of a chip carrier 100 and less than the thickness of the wall material 202. For example, the depth of the grooves may be less than 10 mils thick. The spacing between the grooves 204 may be selected based on design requirements, such as the thickness of the platelets 404, the number of platelets 404 in a completed cube 500, and an allocated space limitation (see Fig. 5). For example, the allocated space limitation may be the size of an infrared sensor that contains a completed cube 500. Any etching technique that is compatible with the chosen wall material 202 may be used. A standard wet etch or plasma etch process that can produce a substantially straight wall trench may be suitable for this purpose.

Fig. 3 is an illustration of an exemplary embodiment of a slotted file 300. A slotted file 300 may consist of two side walls 302 and a back wall 304. Other embodiments may have additional walls. For example, a front wall, a top, or a bottom may also be part of the slotted file 300. The two side walls 302 may be etched with grooves 204. The back wall 304 may be a section of the wall material 202 that has not been etched with grooves 204. The dimensions of the slotted file 300 are based on the size of the platelets 404, the number of platelets 404 that will be placed in the slotted file 300, and the spacing between the platelets 404 in the slotted file 300 (see Fig. 4).

The back wall 304 may be connected to an end of each of the two side walls 302

to form a "U" shape. The grooves 204 on the two side walls 302 face directly across from each other. The three walls 302, 304 may be joined together by conventional methods to form a slotted file 300. For example, an etching process in which tabs and holes are created to join the walls may be employed.

Fig. 4 is an illustration of the stacking process in an exemplary embodiment. The semiconductor chip 108 is placed into the chip carrier 100 to form a platelet 404. For example, the platelet 404 may be less than 5 mils thick. Platelets 404 are then fitted into the slotted file 300 by inserting the flanges 106 into the opposing grooves 204. This may be accomplished by placing the platelet 404 in the vicinity of the opposing grooves 204 and using a shake table to slide the platelet into the opposing grooves 204. The spacing between the platelets 404 is maintained by the groove interval and no pressure is required to hold the chips in place because of the rigidity of the slotted file 300.

Fig. 5 illustrates the completed cube 500 after the platelets 404 have been inserted into the slotted file 300. By using a slotted cube arrangement, the platelets 404 are uniformly stacked without damage. There may be, for example, two hundred platelets 404 in the completed cube 500. The completed cube 500 may be made permanent by immersing the assembly in epoxy. To enable the epoxy to flow between substantially all the layers, the completed cube 500 may be placed in a vacuum chamber. Applying a hard vacuum to the chamber may force the epoxy through substantially all the cracks and layers.

It should be understood that the illustrated embodiments are exemplary only, and should not be taken as limiting the scope of the present invention.